(a) the sense amplifier having respective sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

[(d)] (b) power supply means for providing full high and full low logic level voltages,

[(e)] (c) a pair of field effect transistors, one being a P-channel enhancement mode type having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other being an N-channel enhancement mode type having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

[(f)] (d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.

Claim 7, line 1, after "(DRAM)" insert --as defined in claim 1--.

R E M A R K S

Applicant thanks the Patent Office for allowing claims 1-5 and 10-17.

Parent claims 6 and 7 of the claims rejected under 35 U.S.C. 102(e) have been made dependent from allowed claim